Gurukul International Multidisciplinary Research Journal (GIMRJ)*with* International Impact Factor 8.357
Peer Reviewed Journal
https://doi.org/10.69758/GIMRJ/2504I5VXIIIP0001

e-ISSN No. 2394-8426
Monthly Issue
APR-2025
Issue–IV, Volume–XIII

Design of Digit Serial FIR Filter

Prof. Abhijit Gajendra Kalbande
Assistant Professor
Prof Ram Meghe College of Engineering & Management, Badnera-Amravati
abhijit.g.kalbande@gmail.com

Dr.Saurabh Ashok Ghogare
Assistant Professor,
Adarsha Science J.B.Arts& Birla commerce Mahavidyalaya Dhamangaon Rly.
saurabh.a.ghogare@gmail.com

Abstract- Today filter is the most important component in digital signal processing system from last few decade, on low complexity bit-parallel multiple constant multiplication (MCM) more efficient algorithm and architecture has been developed which are used in DSP system but it offer more complexity as compared to digit serial MCM filter due to which we are interested in design of digit serial MCM filter it has low cost and offers more delay. In this paper we address more the problem of optimizing the area required for to design filter and also we introduce high level synthesis algorithm and overall design architecture. In that experimental result of digit serial FIR MCM filter will be given in term of the area, delay and power efficiency for different algorithm and architecture.

Keywords: -*integer linear programming (ILP), digit serial arithmetic, finite impulse response ((FIR) filters, gate level area optimization, multiple constant multiplication.*

Introduction

In signal processing, a filter is device or process that remove a signal some unwanted component. Filtering is a class of signal processing the defining feature of filtering the complete or partial suppression of some aspect of signal. There characteristics in linear phase and feed forward implementation make them very useful for building stable high performance filter Basically that filter are classified in two type according to their output response i;e finite impulse response filter (FIR) filter & infinite impulse response filter(IFIR) filter, but practically we are not able to design the infinite impulse response filter, so we are interested to design FIR filter. Then depending on the behavior of applied input that FIR will classify in two types i; e parallel fir filter and serial fir filter. In that we are interested in design of serial digit fir filter. Generally fir filter will implemented in two form that is direct and transpose form, this both the architecture have same complexity in hardware, the transpose form is generally preferred because it has high performance and high efficiency. The simple difference between direct and transpose form is simple change the position of "d flip-flop" the multiplier block of digital FIR filter in its transposed form where the multiplication of filter coefficients with the filter input is realized has significant impact on the complexity and performance of design because large number of constant multiplication is required Which has generally known as multiple constant multiplication (MCM) operation and that operation is also called

as central operation. This is use full in DSP system such as fast Fourier transform, discrete cosine transform (DCTs) and error correcting codes. There is full flexibility of multiplier is not necessary for constant multiplication due to which filter coefficient are fixed and it is to be determined by using DSP algorithm .in multiplier multiplication of filter coefficient and input data take place, this type of multiplication is to be implemented using shift add architecture in which each constant multiplication is realized using addition/subtraction and shift operation in MCM block.

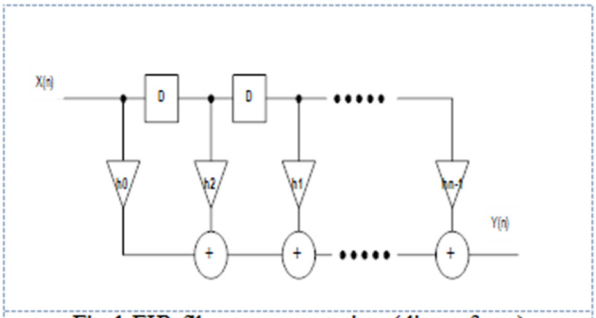

Fig.1.FIR filter representation (direct form)

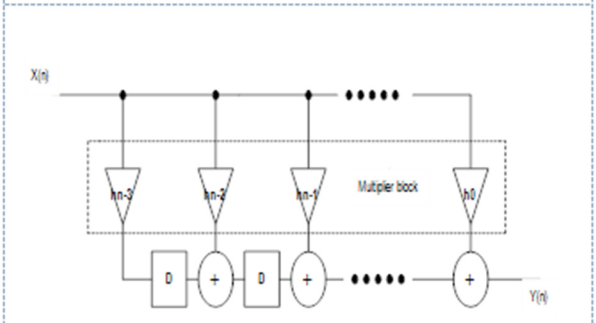

Fig.2.FIR filter representation (transpose form)

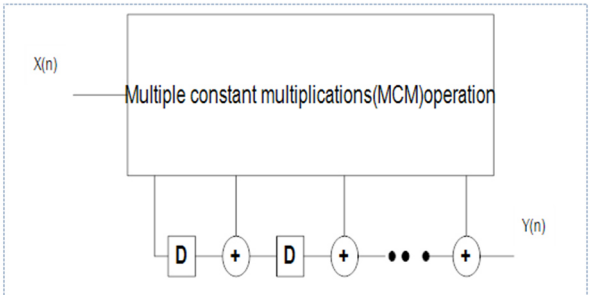

Fig.3.FIR filter representation (direct form with MCM block)

For the implementation of shift adds implementation digit based recording method is used, in that initially it define the constant in binary the for each"1" in the binary representation of the constant , according to bit position it shift the variable and adds up the shifted variables to obtained the result , for going in detail

Gurukul International Multidisciplinary Research Journal (GIMRJ)*with* International Impact Factor 8.357
Peer Reviewed Journal
https://doi.org/10.69758/GIMRJ/2504I5VXIIIP0001

e-ISSN No. 2394-8426
Monthly Issue
APR-2025
Issue–IV, Volume–XIII

we will assume a certain example, consider multiplication 29x and 43x there decomposition in binary are given as

29x = (11101) bin x=x<<4x+ <<3x+ <<2x+x;

43x = (101011) bin x=x<<5x+ <<3x+ <<1x+x;

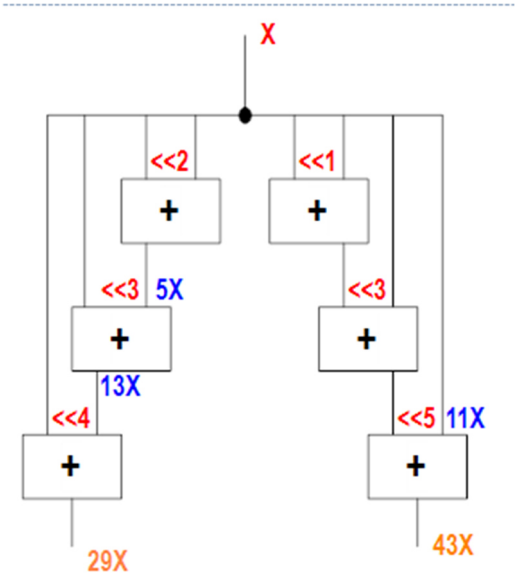

Fig. 4. Shift-adds implementations of 29*x* and 43*x* Without partial product sharing and with partial product sharing

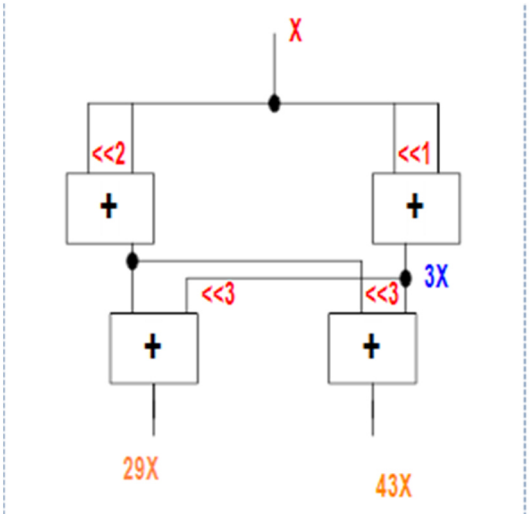

Fig. 5. Shift-adds implementations of 29*x* and 43*x* WithExact CSE algorithm

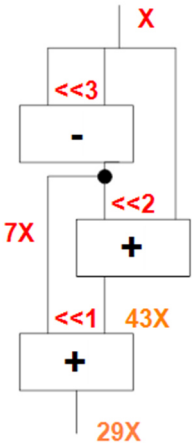

Fig. 6. Shift-adds implementations of 29*x* and 43*x* WithExact Exact GB algorithm.

However, the digit-based recoding technique does not exploit the sharing of common partial products, which allows great reductions in the number of operations and, consequently, in area and power dissipation of the MCM design at the gate level. Hence, the fundamental optimization problem, called the MCM problem, is defined as finding the minimum number of addition and subtraction operations that implement the constant multiplications. Note that, in bit-parallel design of constant multiplications, shifts can be realized using only wires in hardware without representing any area cost. In this paper, we initially determine the gate-level implementation costs of digit-serial addition, subtraction, and left shift operations used in the shift-adds design of digit-serial MCM operations. Then, we introduce the exact CSE algorithm that formalizes the gate-level area optimization problem as a 0–1 integer linear programming (ILP) problem constants are defined under a particular number representation. We also present a new optimization model that reduces the 0–1 ILP problem size significantly and, consequently, the runtime of a generic 0–1 ILP solver. Since there are still instances which the exact CSE algorithm cannot handle, we describe the approximate GB algorithm that iteratively finds the "best" partial product which leads to the optimal area in digit-serial MCM design at the gate level. This paper also introduces a computer-aided design (CAD) tool called SAFIR which generates the hardware descriptions of digit-serial MCM operations and FIR filters based on design architecture and implements these circuits using a commercial logic synthesis tool. In SAFIR, the digit-serial constant multiplications can be implemented under the shift adds architecture, and also can be designed using generic digit serial constant multipliers. The overall result of serial digit fir filter is to check in term of area , delay and power dissipation in term of many specification.

Literature Review: -

2.1. C.Wallace "A suggestion for a fast multiplier,"

THEORY DETAIL:-

It is suggested that the economics of present large-scale scientific computers could benefit from a greater investment in hardware to mechanize multiplication and division than is now common. As a move in this direction, a design is developed for a multiplier which generates the product of two numbers using purely combinational logic,

OUR FINDING:-

From this paper we get information regarding with the design of multiplier, here we are design the filter in that filter required d flip-flop, multiplier, and adder ,but in that multiplier required more hardware as compared to adder/subtractor, so from this paper We get the information regarding to design of fast multiplier.

2.2. W. Gallagher and E. Swartzlander

"High radix booth multipliers using reduced area adder trees,"

THEORY DETAIL:-

The Reduced Area multiplier, the Wallace multiplier, and the Dadda multiplier each offer fast multiplication of signed binary numbers with the use of a large adder tree and a carry look ahead adder. However, their complexity makes them undesirable for some applications. Booth Multiplier, on the other hand, offers Simplicity and flexibility, by both breaking a multiplication up into pieces,and by allowing the size of the pieces to be chosen.

OUR FINDING:-

In this paper we get an idea of to design a multiplier in different way, as we all ready know that for to design multiplier we required more hardware as compared to adder circuit so here in that multiplier is design in a pattern of adder tree that is addition will Take place by using repetitive addition techniques which required less hardware.

2.3. James McClellan, Thomas w parks, Lawrence r rabinar.

"Computer program for designing optimum fir linear phase digital filter."

THEORY DETAIL:-

This paper presents a general-purpose computer program which is capable of designing a large class of optimum (in the minimax sense) FIR linear phase digital filters. The program has options for designing such standard filters also low pass; high-pass, band pass, and band stop filters, as well as multi pass band-stop band filters, differentiators, and Hilbert transformers. The program can also be used to design filters which approximate arbitrary frequency specifications which are provided by the user.

OUR FINDING:-

A general-purpose linear phase FIR filter design Program is presented which is capable of designing a wide variety of standard filters as well as any desired magnitude response which can be specified by the user. The speed of the algorithm, as well as its generality, makes this program an attractive one for a wide variety of design applications.

2.4 H. Nguyen and A. Chatterjee "Number-splitting with shift-and-add decomposition for power and hardware optimization in linear DSP synthesis."

THEORY DETAIL:-

Most DSP synthesis tools perform limited architectural transformations to optimize hardware and power. Multiplications are often implemented with shift-and-add operations for hardware efficiency. In this paper, we propose an optimization that combines a numerical transformation called number-splitting with a shift-and-add decomposition scheme. The numerical transformation "globally" changes the constant multipliers and the data flow-graph of the system under design, enabling implementations with fewer shifts and adds.

OUR FINDING:-

Linear systems are an important class of systems used extensively in engineering and scientific applications. In this paper, we have presented an optimization framework based on numerical techniques. Our optimization methods are based on the premise of real-number splitting and shift-and-add

decomposition for Subexpression sharing. For two's complement encoding of coefficients, the number of operations can be reduced as much as 70%; for more efficient CSD encoding, there was an average 50% saving in operations and 40% in power.

2.5 R. Hartley

"Subexpression sharing in filters using canonic signed digit multipliers,"

THEORY DETAIL: -

Common way of implementing constant multiplication is by a series of shift and adds operations. As is well known, if the multiplier is represented in Canonical Signed Digit (CSD) form, then the number of additions (or subtractions) used will be a minimum This paper examines methods for optimizing the design of CSD multipliers, and in particular the gains that can be made by sharing Subexpression.

OUR FINDING:-

In this paper we get information,The technique of Subexpression sharing has the potential of effecting significant savings in the numbers of additions used in the implementation of FIR filters. The algorithm described an algorithm based on finding common sub-expressions in the CSD representation of the filter coefficients, which can decrease the number of adders by about 50%.

2.6 I.-C. Park and H.-J. Kang,

"Digital filter synthesis based on minimal signed digit representation,"

THEORY DETAIL:-

As the complexity of digital filters is dominated by the number of multiplications, many works have focused on minimizing the complexity of multiplier blocks that compute the constant coefficient multiplications required in filters. The complexity of multiplier blocks can be significantly reduced by using an efficient number system. Although the canonical signed digit representation is commonly used as it guarantees the minimal Number of additions for a constant multiplication**.**

OUR FINDING:-

From this paper we give a new digital filter synthesis algorithm that is based on the MSD representation. Starting from the CSD representation, all the MSD representations are discovered by repeatedly applying simple transforms.

Proposed Work:-

Basically here in this paper our main aim is to design serial digit FIR filter and generally there are two type of filter that is finite impulse response and infinite impulse response but in that we are not able to design infinite impulse response filter practically, so here we are interested in to design of finite impulse response filter . Then according to the way of applied input we can apply input in two ways that is serial and parallel, but in parallel design we required more area and power so we are avoid that disadvantages by designing the serial FIR filter. Again on the basis of applied input we can apply the input in two way i; e bit and digit. It means we can apply input as bit by bit or by using digit. But by referring the reference paper we got that while applying input in bit wise has certain disadvantages, for to avoid it we are applying the input digit wise that is the grouping of number of bit. So overall name of our topic is digit serial fir filter .so for to design the digit serial FIR filter we are distribute overall process in certain step which are as given below.

1. At first we design simple fir filter in direct form without any modification and check the result in term of area, power dissipation and delay.
2. Then we design simple fir filter in direct form without any modification and check the result in term of area, power dissipation and delay.
3. Then perform certain modification in term of adder and multiplier circuit required for the design of digit serial fir filter.
4. Then check the result of serial digit fir filter in term of area, power and delay.

5. Compare all the result of different filter with each other and make a comment that why our design serial digit filter is better as compared to other.

Conclusion

In this paper we are explain different type of filter, on the basis of different specification we are compare them such as an according to area, power dissipation , delay and by comparing all of them we got certain conclusion which is that digit serial FIR filter which is design in our paper is excellent among all the filter.

Reference: -

[1] C. Wallace, "A suggestion for a fast multiplier," IEEE Trans. Electron. Comput, vol. 13, no. 1, pp. 14–17, Feb. 1964.
[2] W. Gallagher and E. Swartzlander, "High radix booth multipliers using reduced area adder trees," in Proc. Asilomar Conf. Signals, Syst. Comput.,vol. 1. Pacific Grove, CA, Oct.–Nov. 1994, pp. 545–549.
[3] J. McClellan, T. Parks, and L. Rabiner, "A computer program for designing optimum FIR linear phase digital filters," IEEE Trans. Audio Electroacoust., vol. 21, no. 6, pp. 506–526, Dec. 1973.
[4] H. Nguyen and A. Chatterjee, "Number-splitting with shift-and-add decomposition for power and hardware optimization in linear DSP synthesis," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 8,no. 4, pp. 419–424, Aug. 2000.
[5] R. Hartley, "Subexpression sharing in filters using canonic signed digit multipliers," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 43, no. 10, pp. 677–688, Oct. 1996.
[6] I.-C. Park and H.-J. Kang, "Digital filter synthesis based on minimal signed digit representation," in Proc. DAC, 2001, pp. 468–473.
[7] L. Aksoy, E. Costa, P. Flores, and J. Monteiro, "Exact and approximate algorithms for the optimization of area and delay in multiple constant multiplications, " IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 27, no. 6, pp. 1013–1026, Jun. 2008.
[8] A. Dempster and M. Macleod, "Use of minimum-adder multiplier blocks in FIR digital filters," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 42,no. 9, pp. 569–577, Sep. 1995.
[9] L. Aksoy, E. Costa, P. Flores, and J. Monteiro, "Optimization of area in digital FIR filters using gate-level metrics," in Proc. DAC, 2007, pp. 420–423.
[10] L. Aksoy, C. Lazzari, E. Costa, P. Flores, and J. Monteiro, "Optimization of area in digit-serial multiple constant multiplications at gate-level," in Proc. ISCAS, 2011, pp. 2737–2740.